

Figure 1 shows a schematic diagram of a system architecture. The diagram illustrates a central processing unit (CPU) connected to a memory unit (MEM) and a storage unit (STG). The CPU is connected to the MEM via a bus system. The MEM is connected to the STG via a bus system. The STG is connected to a network (NET) via a bus system. The NET is connected to a user (USER) via a bus system. The USER is connected to the CPU via a bus system. The CPU is connected to the MEM via a bus system. The MEM is connected to the STG via a bus system. The STG is connected to the NET via a bus system. The NET is connected to the USER via a bus system. The USER is connected to the CPU via a bus system.

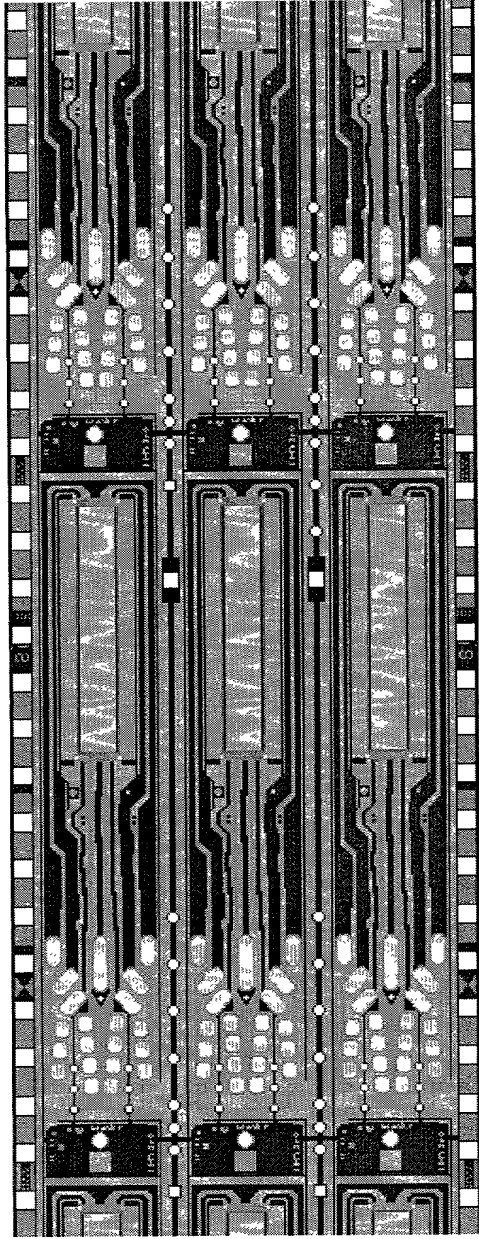


Figure 1

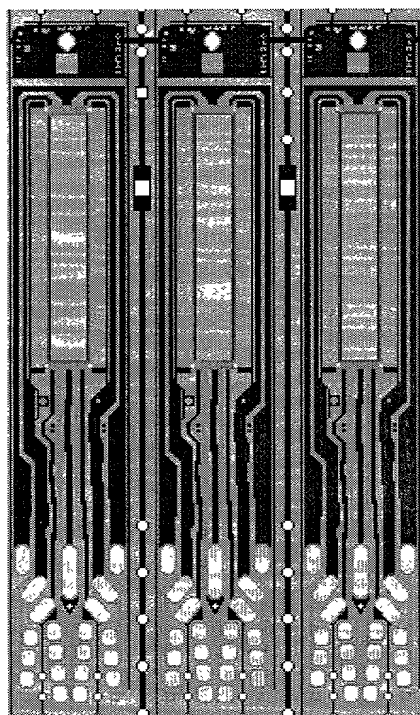


Figure 2